MOSGATED DEVICE WITH ACCUMULATED CHANNEL REGION AND SCHOTTKY CONTACT

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/405,756, filed August 22, 2002.

FIELD OF THE INVENTION

[0002] This invention relates to semiconductor devices and more specifically to a trench type device with on conduction through an accumulated channel region.

BACKGROUND OF THE INVENTION

[0003] Vertical conduction devices in which on state conduction is through an accumulated channel region are well known. U.S. Patent 6,580,123 dated June 17, 2003 in the name of Naresh Thapar (IR-1799) and assigned to the assignee of the present invention shows such a device.

[0004] Figure 1 shows two adjacent cells of such a prior device in cross-section. The device of Figure 1 comprises an N^+ substrate 10 which has an N^- epitaxially deposited drift region 10a and base region 11. A high concentration source region diffusion 12 is formed on the top of epitaxial region 11. The side walls of each of trenches 13 are lined with a gate oxide 14, a bottom oxide TBO 15, and top isolation oxide tox, iso 16. A top source contact 20 contacts N^+ source region 12 and a bottom drain contact 21 contacts the bottom of N^+ substrate 10. Conductive P type polysilicon gates 30 fill the oxide lined trenches 13 and 14 respectively.

[0005] On state conduction in the device of Figure 1 takes place through the accumulated channel region along the silicon mesa walls within N^- channel region 11 which are lined with the gate oxide 13. The device is turned off by shorting the P type gates 30 to the source contact, which depletes out the N^- channel region 30. Further, during blocking most of the charge in the N^- drift region 10a is coupled to the gate so that C_{oss} is almost identical to C_{rss}.

[0006] This type device has several benefits. For example, it has a zero Q_{rr} since there is no body diode, as in a conventional vertical conduction MOSFET. Further, it can have a lower RA, using a sub micron cell pitch. The device can be manufactured with a 4 mask process with no critical alignments. Further, the device has bidirectional capability.

[0007] In order to block voltage, the device needs the P type gate 30 with a base resistivity for N^- base 11 of about 5 ohm-cm resistivity or higher. Sub-micron mesa widths (the distance between adjacent trenches 14) are needed to obtain complete depletion of the N^- channels 11 during turn-off.

[0008] As a result of this structure, the threshold voltage V_{th} is, theoretically about 780 mV and is independent of gate oxide thickness for gate oxide 14.

[0009] A limitation found with the above structure is "snap-back" in the BV_{DSS} characteristics. This snap back was observed between 8 to 22 volts, depending on the thickness of region 11. It is believed that this snap-back occurs because thermally or avalanche generated holes are back-injected into the source, leading to the injection of electrons from the source 20 into the N^- drift region 10a.

BRIEF DESCRIPTION OF THE INVENTION

[0010] In accordance with the invention, a Schottky barrier device is integrated into the silicon containing the MOSFET device to enable collection of avalanche or thermally generated holes to reduce the back injected hole current into the N^+ source region thus averting the BV_{DSS} snapback. The Schottky barrier can be

integrated anywhere in the chip but is preferably located immediately adjacent to and within the N^+ source region. A dual gate structure and/or a source contact trench can be added to further control device V_{th} and to improve light load efficiency.

[0011] In forming the Schottky contact, any desired Schottky barrier can be used. Good results have been obtained with Aluminum as the barrier. A novel geometry is provided to produce a relativity large area Schottky contact by forming the contact in and along the walls of a trench which extends through the N^+ source layer and into the N^- base region.

[0012] A novel process is also provided for forming the P type gate. Thus, the gate trench is first formed and is then lined with polysilicon. This polysilicon is then implanted with a P type impurity, for example, boron. The trench is then completely filled with polysilicon and the implant is activated. This process has the advantage of a limited thermal cycle and produces a deeper penetration of boron into the polysilicon gate than is obtained by the heavier boron implant into a filled polysilicon mass in the trench.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figure 1 is a cross-section of a small portion of a prior art device.

[0014] Figure 2 shows Figure 1 with an added Schottky diode integrated into the device silicon in accordance with the invention.

[0015] Figure 3 is a cross-section of Figure 2 to show the locations of the Schottky contacts between plural cells.

[0016] Figure 4 shows a half cell cell of a device of the invention with preferred dimensions for the cell.

[0017] Figure 5 shows band diagrams which illustrate the hole collection without barrier via the Schottky are of the device of Figure 2.

[0018] Figure 6 shows the device of Figure 2 wherein the gates are separately controlled as a dual gate device to permit V_{th} control.

[0019] Figure 7 shows a reversed source-drain device with the dual gate structure of Figure 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0020] Referring first to Figure 2, 3, 4 and 5, the elements of those devices which are similar to those of Figure 1 have the same identifying numeral.

[0021] In Figure 2, the source region 12 has a laterally projecting region of any desired shape which contains spaced openings such as openings 40 (Figure 3) of any desired shape through which the aluminum source contact 20 (or any other Schottky-forming metal) can project to contact base 11 and form a Schottky diode.

[0022] Figures 3 and 4 show the use of aluminum layers 50 as the Schottky forming barrier. Other Schottky barrier layer segments could be used. The opening 40 through the N^- layer 12 may have any desired geometry, and such openings may be distributed over at least a major portion of the area of the N^+ source region 11 as shown in Figure 3.

[0023] The modified structure of Figures 2, 3 and 4 achieves the following:

1. The source metal 20 on top of the N^+ source region 12 adjacent cross-section makes ohmic contact to the N^+ source region 12. However, a Schottky contact is made to the N^- base region in the third dimension is indicated in Figure 2.

2. This enables avalanche or thermally generated holes to be laterally collected by the Schottky contact and reduces the back-injected hole current into the N^+ source region 12 thus averting the BV_{DSS} snapback of the structure of Figure 1.

[0024] Figure 4 shows a single cell made according to the schematic diagrams of Figures 2 and 3. Figure 4 shows the dimensions which can be used in the preferred embodiment of the invention. Note that the Schottky barrier in Figure

4 is formed in a shallow trench 60 in the N^+ source region 12 and into the N^- base region. A thin Schottky barrier is formed by an enlarged area layer lining the sides and bottom of trench 60 and is contacted by the aluminum source contact 20 which also contacts the source region 12 as shown. The insulation layer 16 atop the gate is a silicon dioxide layer with a side wall spacer portion 16a.

[0025] A preferred method for forming the P type gate polysilicon includes the process steps of etching trenches 13 (and 16) and thereafter depositing a thin layer of polysilicon over the walls of trench 13. Thereafter, the deposited polysilicon receives a heavy boron implant. The remainder of the trench is then filled with undoped polysilicon and the boron implant is then activated, distributing the P charge throughout the polysilicon filler.

[0026] The structure of Figure 4 is conceptually similar to that of Figure 2 except that the Schottky can be formed without the need for an extra mask level. Further, V_{th} is higher, dependent on gate oxide (tox, g) due to the band bending caused by the built-in potential of the Schottky contact to the N^- base region. Both of these limitations are addressed while still retaining the original feature of the accumulation channel region device of having zero Qrr as in the device of Figures 1, 2 and 3.

[0027] Further, the device of Figure 4, has improved EAS capability and has an increased Schottky conduction area. The half cell pitch in Figure 4 is about 0.55μm.

[0028] Figure 5 is a metal-semiconductor band diagram for an ideal Schottky diode to explain the operation of the device of Figures 2, 3 and 4. The diagram shows that holes will be collected from the N base 11 to the metal 20. That is, holes will be collected from the N base 11 to the Schottky metal 20 but will not be injected from the Schottky metal 20 to the base 11, thereby retaining the feature of no minority carrier (hole) injection into the N^- base region 11.

[0029] Figure 6 shows a further embodiment of the device of Figure 3 in which gates 13 and 14 are separately controlled from terminals G1 and G2, rather

than being simultaneously energized as in Figures 1, 2, 3 and 4. The separation of the gates enables V_{th} control while retaining the benefit of the integrated Schottky diode.

[0030] More specifically in Figure 6;

1. During turn-on only gate G_1 is biased +ve with respect to source. Gate G_2 is shorted to the source. Using P-type gates, as in a conventional Accufet™ device structure a higher gate G_1 bias is needed to undo the band bending caused by gate G_2 along the trench sidewall controlled by gate G_1. This enables the V_{th} of the channel controlled by gate G_1 to be determined by the gate oxide along the trench sidewall of gate G_1.

2. All such dual gate devices can be designed to have greater light load efficiencies. Basically, at light loads where the switching losses dominate, only the channel controlled by gate G_1 will be used thereby reducing the switching losses in half and at high loads, where conduction losses dominate, both the channels controlled by gate G_1 and gate G_2 will be used.

[0031] Figure 7 is a cross-section of a cell of a device in which the source an drain of Figures 2 and 3 are reversed and in which the two-gate structure of Figure 6 is employed.

[0032] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.